REMARKS

Claims 1-4, 8-54 and 58-72 are rejected under 35 U.S.C. 102(e) as being anticipated by Ollivier, *et al.* (U.S. Patent Number 6,738,881). Claims 5-7 and 55-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ollivier, *et al.* In view of the amendments to the claims and the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

In the present invention as claimed in claims 1-22, a system for transferring a signal to a channel includes a storage unit associated with the channel for storing source identification information of a plurality of sources. The source identification information indicates an order of priority of the plurality of sources for access to the channel. The system further includes a plurality of selection circuits for receiving input signals from the sources, each of the selection circuits selecting one of the plurality of input signals in response to the source identification information. The system further includes a circuit for checking outputs of the selection circuits and forwarding selected input signals to the channel.

In the present invention as claimed in claims 23-36, a system for transferring signals to channels includes a plurality of storage units, each storage unit being associated with one of the channels, and each storage unit being adapted to store source identification information indicating an order of priority of the sources for access to the channel. The system further includes a plurality of selection circuits for receiving input signals from the sources, each of the selection circuits selecting one of the plurality of input signals in response to the source identification information. The system further includes a circuit for checking outputs of the selection circuits and forwarding selected input signals to the channel.

In the present invention as claimed in claims 37-50, a direct memory access (DMA) controller for controlling transfer of signals from input sources to output devices, a plurality of channels being connected to the output devices, includes a plurality of storage units, each storage unit being associated with one of the channels, and each storage unit being adapted to store source identification information indicating an order of priority of the sources for access to the channel. The system further includes a plurality of selection circuits for receiving input signals from the sources, each of the

selection circuits selecting one of the plurality of input signals in response to the source identification information. The system further includes a circuit for checking outputs of the selection circuits and forwarding selected input signals to the channel.

In the present invention as claimed in claims 51-72, a method of transferring a signal to a channel includes storing source identification information for a plurality of sources. The source identification information indicates an order of priority of the plurality of sources for access to the channel. The method further includes providing a plurality of selection circuits for receiving input signals from the sources, each of the selection circuits selecting one of the plurality of input signals in response to the source identification information. The method further includes, with a checking circuit, checking outputs of the selection circuits and forwarding a selected input signal to the channel.

Claims 1-72 are amended to clarify that one of the plurality of input signals is selected in response to source identification information indicating an order of priority of the sources for access to the channel, and forwarding the selected input signal to the channel. That is, the order of priority is determined based on the source identification information stored in a storage unit associated with the channel. The source identification information indicates an order of priority of the sources for access to the channel. It is believed that these amendments to the claims clarify the distinctions between the claimed invention and the cited references.

Ollivier, *et al.* discloses that a scheduler scans all the channel descriptor registers (a source descriptor 650, a destination descriptor 652 and enable descriptor 620) and FIFO counters to determine if requests are waiting to be served. Each possible request is given a request identifier. If there are several requests waiting, they are served on a round robin scheme. If request r is the current request served, the next request served will be r+1. In Ollivier, *et al.*, the source descriptor indicates a source of the transfer, the destination descriptor indicates a destination of the transfer, and the enable descriptor indicates whether the channel is enabled or disabled. In determining which request to serve, the channel descriptors are merely scanned in order to determine if requests are waiting to be served. The requests in Ollivier, *et al.* are given identifiers and then are served based on a round robin scheme. Further, in Ollivier, *et al.*, the channel priority PRIO(5:0) field defines the priority of each channel. PRIO[i]=0 indicates channel i has a

low priority; PRIO[i]=1 indicates channel i has a high priority. A HPI priority HPI[1:0] field defines the priority of the host port in relation to the DMA channels. In a given round-robin queue, each channel is switched to the next channel after its read has been triggered. The low priority channels will be pending as long as high priority channels need to be triggered.

Ollivier, *et al.* fails to teach or suggest a system for transferring a signal to a channel which includes a storage unit associated with the channel for storing source identification information of a plurality of sources, a plurality of selection circuits for receiving input signals from the sources, each of the selection circuits selecting one of the plurality of input signals in response to the source identification information which indicates an order of priority of the plurality of sources for access to the channel, and a circuit for forwarding selected input signals to the channel, as claimed in claims 1-22. In addition, Ollivier, *et al.* fails to teach or suggest a system for transferring signals to channels includes a plurality of storage units, each storage unit being associated with one of the channels, and each storage unit being adapted to store source identification information indicating an order of priority of the sources for access to the channel, a plurality of selection circuits, for each or the plurality of channels, for receiving input signals from the sources, each of the selection circuits selecting one of the plurality of input signals in response to the source identification information, and a circuit for forwarding selected input signals to the channel, as claimed in claims 23-36. Further, Ollivier, *et al.* fails to teach or suggest a direct memory access (DMA) controller that includes a plurality of storage units, each storage unit being associated with one of the channels, and each storage unit being adapted to store source identification information indicating an order of priority of the sources for access to the channel, a plurality of selection circuits, for each of the plurality of channels, for receiving input signals from the sources, each of the election circuits selecting one of the plurality of inputs in response to the source identification information, and a circuit for forwarding selected input signals to the channel, as claimed in claims 37-50. In addition, Ollivier, *et al.* fails to teach or suggest a method of transferring a signal to a channel which includes storing source identification information for a plurality of sources, the source identification information indicates an order of priority of the plurality of sources for access to the channel, providing a plurality of selection circuits for receiving input signals from the

sources, each of the selection circuits selecting one of the plurality of input signals in response to the source identification information, and, with a checking circuit, forwarding a selected input signal to the channel, as claimed in claims 51-72.

The source descriptor 650, the destination register 652 and the enable descriptor 654 of Ollivier, *et al.* in no way indicate an order of priority of the plurality of sources for access to the channel. Rather, in Ollivier, *et al.*, the source descriptor indicates a source of the transfer, the destination descriptor indicates a destination of the transfer, and the enable descriptor indicates whether the channel is enabled or disabled. In Ollivier, *et al.*, the order of priority of the sources for access to the channel is not indicated by the source descriptor, the destination descriptor and the enable descriptor. Further, while Ollivier, *et al.* allows for transfer of high priority channels over low priority channels, Ollivier, *et al.* in no way teaches or suggests that input signals from the sources are selected based on the source descriptor, the destination descriptor and the enable descriptor. In the present invention as claimed, one of the plurality of input signals from the sources is selected in response to the source identification information which indicates an order of priority of sources for access to the channel. In Ollivier, *et al.*, while the low priority channels must wait until the high priority channels no longer need to be triggered, there is no selection of inputs from the sources based on source identification which indicates an order of priority of the plurality of sources for access to the channel prior to transfer on the channels.

Ollivier fails to teach or suggest certain elements of the invention set forth in claims 1-22, 23-36, 37-50 and 51-72, as discussed above. Therefore, it is believed that the amended claims are allowable over the cited reference, and reconsideration of the rejections of claims 1-4, 8-54 and 58-72 under 35 U.S.C. 102(e) as being anticipated by Ollivier, *et al.*, and the rejections of claims 5-7 and 55-57 under 35 U.S.C. § 103(a) based on Ollivier, *et al.* is respectfully requested.

In view of the amendments to the claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

In connection with this matter, please charge any otherwise unpaid fees which may be due or credit any overpayment to Deposit Account No. 501798.

Respectfully submitted,

Date: 12/29/08

Mills & Onello, LLP
Eleven Beacon Street, Suite 605
Boston, MA 02108
Telephone: (617) 994-4900
Facsimile: (617) 742-7774
J:\SAM\0442\120208AdvisoryAction\Response_120208AA.doc

Steven M. Mills
Registration Number 36,610
Attorney for Applicants